

LISTING OF THE CLAIMS

Claims 1-2 (Cancelled)

3. (Previously Presented) An adder circuit comprising:  
a first adder cell having:

a first logic gate having a first input that receives a first input signal, a second input that receives a second input signal, and a first output that generates a first logic signal, the first input signal, the second input signal, and the first logic signal each having a logic state, the first logic gate generating the first logic signal in response to the logic states of the first and second input signals, the first logic gate generating an inverted first input signal in response to the first input signal;

a first inverter circuit having a third input that receives a third input signal, a fourth input connected to receive the first logic signal, a first output that generates an inverted third signal, and a second output that generates an inverted first logic signal;

a first carry out circuit having a first control input connected to receive the first logic signal, a second control input connected to receive the inverted first logic signal, and an output, the carry out circuit including a first multiplexer that passes a first received signal to the output of the first carry out circuit when the first logic signal has a first logic state, and passes a second received signal to the output of the first carry out circuit when the first logic signal has a second logic state, the first received signal being the first input signal; and

a first sum circuit having a first control input connected to receive the first logic signal, a second control input connected to receive the inverted first logic signal, a first sum input connected to the third input signal, a second sum input connected to the inverted third signal, and an output, the second sum input and the output of the first sum circuit not be directly connected together.

4. (Cancelled)

5. (Previously Presented) The adder of claim 3 wherein the second received signal is the third input signal.

Claims 6-7 (Cancelled)

8. (Previously Presented) The adder of claim 3 wherein the first sum circuit includes a second multiplexer that passes a third received signal to the output of the first sum circuit when the logic signal has a first logic state, and passes a fourth received signal to the output of the first sum circuit when the logic signal has a second logic state.

9. (Original) The adder of claim 8 wherein the third received signal is the third input signal, an input to the second multiplexer being connected to the first sum input.

Claims 10-11 (Cancelled)

12. (Original) The adder of claim 8 wherein the fourth received signal is the inverted third signal.

13. (Cancelled)

14. (Previously Presented) The adder of claim 3 and further comprising a first buffering inverter having an input connected to the output of the first carry out circuit, and an output.

Claims 15-16 (Cancelled)

AMENDMENT UNDER 37 CFR §1.116,  
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17. (Previously Presented) The adder circuit of claim 3 wherein the output of the first carry out circuit has a first active state; and further comprising:

a second adder cell connected to receive a signal from the output of the first carry out circuit of the first adder cell, the second adder cell having:

a second logic gate having a fifth input that receives a fifth input signal, a sixth input that receives a sixth input signal, and a second output that generates a second logic signal, the fifth input signal, the sixth input signal, and the second logic signal each having a logic state, the second logic gate generating the second logic signal in response to the logic states of the fifth and sixth input signals, the second logic gate generating an inverted fifth signal in response to the fifth input signal;

a second inverter circuit having a seventh input that receives a seventh input signal, an eighth input connected to receive the second logic signal, a first output that generates an inverted seventh signal, and a second output that generates an inverted second logic signal;

a second carry out circuit having a first control input connected to receive the second logic signal, a second control input connected to receive the inverted second logic signal, and a second output, the second carry out circuit including a second multiplexer that passes a third received signal to the output of the second carry out circuit when the first logic signal has a first logic state, and passes the signal from the output of the first carry out circuit to the output of the second carry out circuit when the first logic signal has a second logic state, the second output of the second carry out circuit having a second active state opposite the first active state; and

a second sum circuit having a first control input connected to receive the second logic signal, a second control input connected to receive the inverted second logic signal, and an output.

18. (Previously Presented) The adder circuit of claim 17 and further comprising:

a third adder cell connected to receive a signal from the output of the second carry out circuit of the second adder cell, the third adder cell having:

a third logic gate having an ninth input that receives a ninth input signal, a tenth input that receives a tenth input signal, and a third output that generates a third logic signal, the ninth input signal, the tenth input signal, and the third logic signal each having a logic state, the third logic gate generating the third logic signal in response to the logic states of the ninth and tenth input signals, the third logic gate generating an inverted ninth signal in response to the ninth input signal;

a third inverter circuit having a eleventh input that receives an eleventh input signal, a twelfth input connected to receive the third logic signal, a first output that generates an inverted third signal, and a second output that generates an inverted third logic signal;

a third carry out circuit having a first control input connected to receive the third logic signal, a second control input connected to receive the inverted third logic signal, and a second output, the second output of the third carry out circuit having a second active state; and

a third sum circuit having a first control input connected to receive the third logic signal, a second control input connected to receive the inverted third logic signal, and an output.

19. (Original) The adder circuit of claim 17 wherein the first adder cell is in a first row and the second adder cell is in a second row.

20. (Original) The adder circuit of claim 18 wherein the first adder cell is in a first row, the second adder cell is in a second row, and the third adder cell is in a third row.

Claims 21-22 (Cancelled)

23. (Previously Presented) The circuit of claim 5 wherein the first logic gate is an XOR gate when the first input signal and the second input signal have equivalent signal polarities.

24. (Previously Presented) The circuit of claim 5 wherein the first logic gate is an XOR gate when the first input signal and the second input signal have different signal polarities.

25. (Previously Presented) An adder circuit comprising:  
a first adder cell having:

a first exclusive OR circuit having a first input, a second input, and an output, the output having a logic state that represents an exclusive ORing of a logic state on the first input and a logic state on the second input;

a first output circuit having:

a first transmission gate having first and second transistors connected to an input and an output, the first and second transistors having first and second gates, respectively;

a second transmission gate having first and second transistors connected to an input and an output, the first and second transistors of the second transmission gate having first and second gates, respectively, the outputs of the first and second transmission gates being connected together;

a third transmission gate having first and second transistors connected to an input and an output, the first and second transistors of the third transmission gate having first and second gates, respectively;

a fourth transmission gate having first and second transistors connected to an input and an output, the first and second transistors of the fourth transmission gate having first and second gates, respectively, the outputs of the third and fourth transmission gates being connected together; and

a first inverting circuit having an input connected to the input of the second transmission gate and the input of the third transmission gate, and an output connected to the input of the fourth transmission gate.

26. (Previously Presented) The adder circuit of claim 25 wherein the input of the first transmission gate is connected to the first input of the exclusive OR circuit.

27. (Cancelled)

28. (Previously Presented) The adder circuit of claim 26 wherein the first gates of the first and third transmission gates and the second gates of the second and fourth transmission gates are connected together.

29. (Previously Presented) The adder circuit of claim 28 and further comprising a second inverting circuit having an input connected to the output of the first exclusive OR circuit, and an output connected to the first gate of the first transmission gate.

30. (Previously Presented) The adder circuit of claim 26 and further comprising:

a second adder cell having:

a second exclusive OR circuit having a first input, a second input, and an output;

a second output circuit having:

a fifth transmission gate having first and second transistors connected to an input and an output, the first and second transistors of the fifth transmission gate having first and second gates, respectively;

a sixth transmission gate having first and second transistors connected to an input and an output, the first and second transistors of the sixth transmission gate having first and second gates, respectively, the outputs of the fifth and sixth transmission gates being connected together, the input of the sixth transmission gate being connected to the output of the first transmission gate; and

a second inverting circuit connected to the outputs of the fifth and sixth transmission gates.

31. (Previously Presented) The adder circuit of claim 26 and further comprising

a second inverting circuit having an input connected to the output of the first transmission gate of the first output circuit; and

a second adder cell having:

a second exclusive OR circuit having a first input, a second input, and an output;

a second output circuit having:

a fifth transmission gate having first and second transistors connected to an input and an output, the first and second transistors of the fifth transmission gate having first and second gates, respectively; and

a sixth transmission gate having first and second transistors connected to an input and an output, the first and second transistors of the sixth transmission gate having first and second gates, respectively, the outputs of the fifth and sixth transmission gates being connected together, the input of the sixth transmission gate being connected to the output of the second inverting circuit.

32. (Previously Presented) The adder of claim 31 wherein:

the first exclusive OR circuit includes a third inverting circuit that has an input connected to the first input of the first exclusive OR circuit, and an output; and

the input of the first transmission gate is connected to the input of the third inverting circuit.

33. (Previously Presented) The adder of claim 32 wherein the second exclusive OR circuit includes a fourth inverting circuit that has an input connected to the first input of the second exclusive OR circuit, and an output; and

the input of the fifth transmission gate is connected to the output of the fourth inverting circuit.

## Claims 34-36 (Cancelled)

37. (Previously Presented) The adder circuit of claim 31 wherein the first adder cell is in a first row and the second adder cell is in a second row.

38. (Previously Presented) The adder circuit of claim 37 wherein only first adder cells are in the first row, and none of the first adder cells in the first row are electrically connected together.

39. (Previously Presented) The adder circuit of claim 38 wherein only second adder cells are in the second row, and none of the second adder cells in the second row are electrically connected together.

40. (Previously Presented) The adder circuit of claim 39 and further comprising a third row of adder cells connected to the second row of adder cells, the third row including first and second adder cells.